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LOW POWER DIGITAL DESIGN USING ASYNCHRONOUS FINE GRAIN LOGIC

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Abstract— In this paper, a fine-grained power gating technique for an asynchronous-logic pipeline stage is proposed using locally controlled gating transistors. Pipeline stage in the AFPL circuit is consisting of positive feedback adiabatic logic (PFAL) gates that implement the logic function of the stage, and a handshake controller, that handles handshaking with the neighboring stages and gives power to the PFAL gates. The partial charge reuse (PCR) mechanism can be added in the AFPL circuit. Using the PCR mechanism, part of the charge on the output nodes of a PFAL gate entering the discharge phase can be used to charge the output nodes of another PFAL gate which is more enough to complete evaluate phase, reducing the energy dissipation. AFPL-PCR adopts an enhanced C-element, called C*-element, in its handshake controllers such that an PFAL gate in AFPL-PCR can enter into the sleep mode earlier once the output has been received by the downstream pipeline stage. The proposed power gating technique is implemented with minimal control overheads and the interest in non-synchronous design of digital circuits is growing due to technology scaling into deep submicron transistor geometries.

Keywords— Asynchronous Circuits, Logic Gates, Low-Power Electronics, Power Gating, Partial Charge Reuse.

I. INTRODUCTION

Low power has emerged as a principal theme in nowadays electronics industries. As the parameters like performance and area for VLSI Chip design, Power dissipation becomes an important consideration. With minimizing technology minimizing power consumption and over all power management on chip are the key challenges below 100nm due to increased complexity in the circuits. For power management leakage current also plays a fundamental role in low power VLSI designs.

Leakage current is becoming an increasingly important fraction of the total power dissipation of integrated circuits. With the increasing popularity of battery-driven portable electronic devices, there is a growing demand for low-power circuit designs. Dynamic power dissipation remains to be the most dominant part in many digital circuits. Leakage power dissipation has become increasingly most significant especially when the fabrication process enters into deep-sub-micro- or nano-meter-scaled ranges. Asynchronous circuits are well-known for their benefits in terms of dynamic power savings, because asynchronous logic circuits does not switch when inactive. Moreover, in deep submicron technologies, leakage currents have become an increasing problem , and thus asynchronous circuits need to focus on reducing power consumption.

Various methods for reducing leakage loss in CMOS circuits have proposed both at the circuit and process technology levels. At the circuit level, leakage reduction methods include transistor stacking, reverse body biasing, dual threshold CMOS, and power gating [1]. In these methods, power gating is one of the most effective techniques for leakage reduction. In general, power gating techniques increase the effective resistance of leakage paths by inserting sleep transistors (power gating transistors) between power supply rails and transistor stacks. In the idle (sleep) mode, the sleep transistors are turned off, and it will cut the pull-up and pull-down networks off from one or both power rails, and thus the leakage current is suppressed; in the active mode, the sleep transistors will be turned on, reconnecting the pull-up and pull-down networks to power supply rails. Some implementation methodologies of power-gating techniques include multithreshold CMOS, boosted-gate CMOS, super cut-off CMOS, variable threshold CMOS, and zigzag super cut-off CMOS.

In, each combinational block in the conventional asynchronous four-phase bundled-data pipeline is made up of both a header and a footer sleep transistor. When the latch controller in a pipeline stage detects valid input data, it absorbs the data in the data latch and turns on the sleep transistors of the associated combinational block, so that the combinational block will wake up and processes the input data and generates the output data[2]. When the output data

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are Received by the next pipeline stage, an acknowledge signal is sent back to this stage, and the latch controller can turn off the sleep transistors of the associated combinational block to reduce leakage dissipation. Moreover this scheme has the certain disadvantages. First one, the hardware overhead is large. Each combinational block requires a standalone data latch, a complex latch controller consisting of six logic gates and two C-elements, two sleep transistors, and an inverter chain for matching delay. Second one, only the combinational blocks can be power-gated [3], all other hardware, including data latches, latch controllers, and inverter chains, will still suffer leakage dissipation. In, asynchronous adiabatic logic (AAL), each stage in an AAL circuit consists of an adiabatic gate, which implements the logic function of that stage, and a control and regeneration (C&R) block, whose output supplies power to the associated adiabatic logic gate.

When the C&R block detects that the input to the adiabatic gate becomes valid, the output of the C&R block transits to HIGH, and the adiabatic gate can acquire power to evaluate its output; when the C&R block detects that the input to the adiabatic gate becomes empty, the output of the C&R block transits to LOW, and the adiabatic gate is not powered and becomes idle [4]. The synchronization between neighboring stages in an AAL circuit is accomplished via a unidirectional control signal (i.e., the output of the C&R block) rather than bidirectional handshake signals, so an AAL circuit whose pipeline stages have diverse propagation delay may cause a data token propagating along the pipeline to be overridden by its succeeding data token. An innovative way to reduce power consumption by low-power logic family, called asynchronous fine-grain power-gated logic (AFPL). Here, power consumption of proposed system is compared with conventional system.

II. AFPL - OVERVIEW

AFPL can be combined with the PCR mechanism. When AFPL adds the PCR mechanism, it is denoted by AFPL-PCR, otherwise, it is denoted by AFPL w/o PCR.[Fig. 1] shows the structure of the AFPL pipelines. In AFPL w/o PCR], a pipeline stage, denoted by S_i , is comprised of an efficient charge recovery logic (ECRL) gate G_i, which implements the logic function of the stage, and a handshake controller HC_i , which handles handshaking [6] with the neighboring stages and provides power to ECRL logic gate G_i In AFPL-PCR [Fig. 1] a pipeline stage, denoted by S_{i+1}, has an additional unit, the PCR unit PCR_{i+1}, which maintains charge reuse between pipeline stages S_i and S_{i+2}..

An asynchronous system was made up of many autonomous modules, each of which operates at its own rate and communicates with its neighboring modules only when it wants to exchange information. The synchronization between those autonomous modules was not achieved by a global clock but rather by local handshake signals, request and acknowledge. The handshake protocol used in the AFPL pipeline is the four phase dual-rail protocol, in which the request signal is encoded into the data signals (i.e., there is no separate request signal) and n pairs of wires are required to encode n-bit data. The transferring of data from the sender to the receiver involves the following four actions:

- The sender issues a valid codeword on the communication channel
- The receiver acquires the valid codeword from the communication channel, and then asserts the acknowledge signal.
- The Sender responds by issuing an empty codeword (i.e., taking all data wires low) to indicate that the data on the communication channel is no longer valid.
- The receiver desserts the acknowledge signal to complete the communication cycle. Thus, the data stream flowing through the handshake controllers instead of the conventional fixed dc power supply

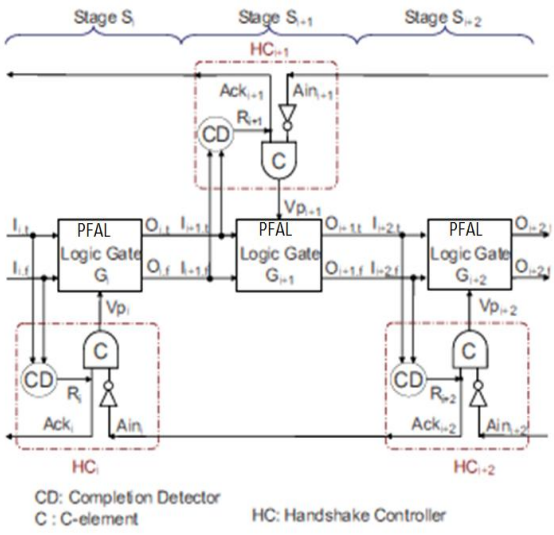

Fig1 : Block diagram of AFPL without PCR

CD: Completion detector
HC: Handshake controller
C : C-Element

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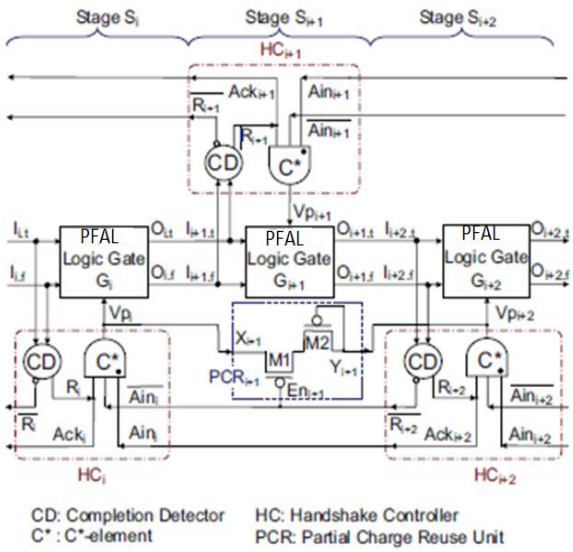

Fig 2 : Block diagram of AFPL-PCR

III. PFAL

PFAL like IECRL is also based around a pair of cross coupled inverters. However, whilst in IECRL the NMOS devices used to evaluate the function are connected between the outputs and ground, in PFAL, these evaluation NMOS devices are connected between the outputs and the power-clock. The similarities between PFAL and IECRL gates are such that IECRL gates can be easily converted into PFAL gates. This is done by re-labelling the outputs so that their assertion levels are swapped [7], and connecting the NMOS evaluation devices between the power-clock and the outputs rather than between ground and the outputs. This can be made as easy to achieve in layout as it is in abstract representations of the circuit. When the power-clock is in its recovery phase, the NMOS devices between the outputs and the power-clock can allow complete recovery of those outputs.

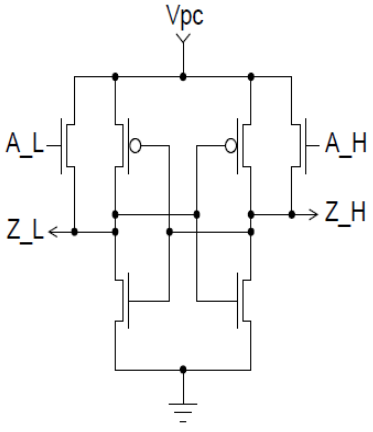

Fig 3 : PFAL logic

IV. HANDSHAKE CONTROLLERS AND FINE-GRAIN POWER-GATING

In the AFPL pipeline, the handshake controller HC_i in stage S_i performs the following tasks:
detecting the validity of the inputs to the PFAL logic gates in stage S_i offering power to the PFAL logic gates in stage S_i detecting whether the outputs of stage Si have been received by the downstream stage S_{i+2} informing the upstream stage S_{i-2} when S_{i-2} can remove its outputs

A handshake controller is comprised of a completion detector (CD), a C-element and an inverter. The CD in HC_i is used to detect whether the input to stage Si represents a valid codeword or an empty codeword. The output of the CD transits from low to high [8].when the input to stage si becomes a valid codeword, and transits from high to low when the input to stage Si becomes an empty codeword. If the input consists of n-bit data, n pairs of wires are required to encode the input, and the associated CD can be implemented with a n-input C-element gate and n two-input OR gates.

The output of the C-element in HC_i is connected to V_{pi}, the power node of the PFAL gates in stage Si shows the structure of the C-element used in AFPL w/o PCR. C-element gate is a state-holding device, and its output is set to high when all inputs are high and set to low when all inputs are low. When the AFPL circuit starts up, the Reset signal is used to initialize the outputs of all C-elements in AFPL to low and thereby all power nodes are set to 0 V. That is, every stage in the AFPL pipeline operates in the wait phase in the beginning. The input data stream for the AFPL pipeline is a sequence of alternating valid and empty tokens. A valid/empty token at the input end of the pipeline will propagate along the pipeline stages and eventually appear at the output end.

V. PCR MECHANISM AND ENHANCED C-ELEMENT

There are two main differences between AFPL-PCR and AFPL w/o PCR. First, AFPL-PCR consists of PCR unit PCR_{i+1} to control charge reuse between pipeline stages Si and S_{i+2}. Second one [9], the handshake controller HCi in AFPL-PCR employs an enhanced C-element, called C-element and to control the power node Vpi of the associated PFAL gates. The C □-element has the advantage that a PFAL gate can achieve early discharging if its outputs are no longer required, without waiting for the next empty token to arrive at this stage. In the PCR_{i+1} unit, transistor M2 is used as a diode, the M2 transistor allows the current to flow only

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in the direction from Vpi to V_{pi+2}, and transistor M1 is used as a switch, which is turned on when charge reuse is activated [10] [11].

The C -element in HCi has three inputs, Ri, A_{ini}, and A_{ini} , the latter two of which are complementary. Ri is the request signal from the CD in HCi. A_{ini} and A_{ini} are the acknowledge signals from HC_{i+1}. After reset, Ri = 0, A_{ini} = 0, and A_{ini} = 1.

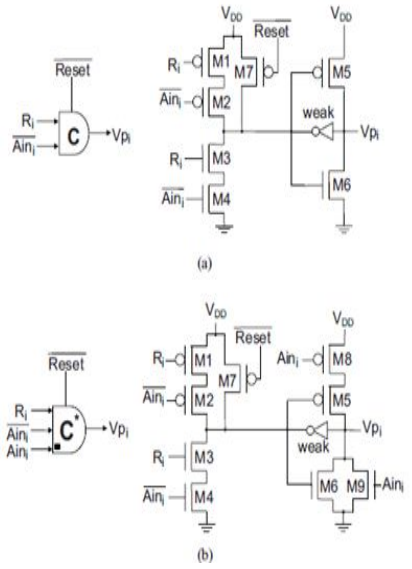

Fig 4 : Structure of C- element used in AFPL

VI. SIMULATION RESULTS

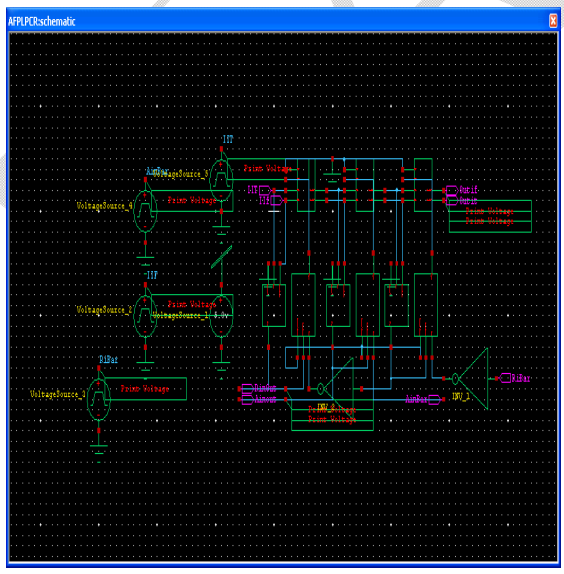

Fig 5: Circuit schematic of AFPL

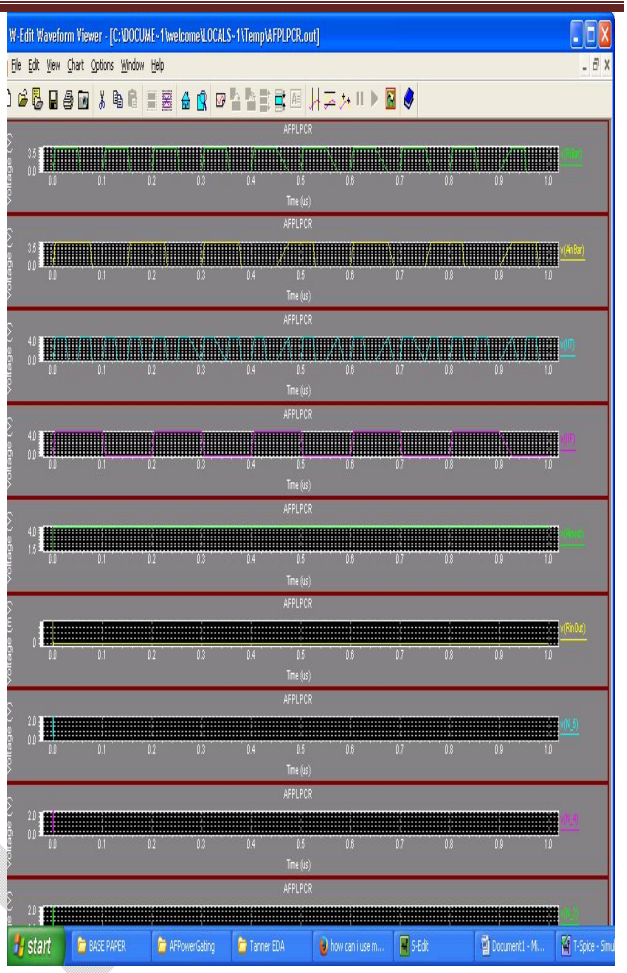

Fig 6 : Output waveform
Input and output voltage in volts with respect to time in Microseconds .of Asynchronous Fine Grain Power Gated Logic(AFPL)

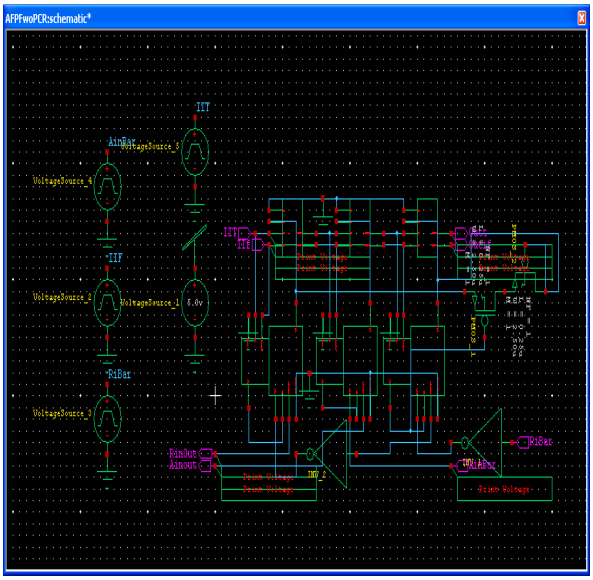

Fig 7 : Circuit schematic of AFPL- PCR

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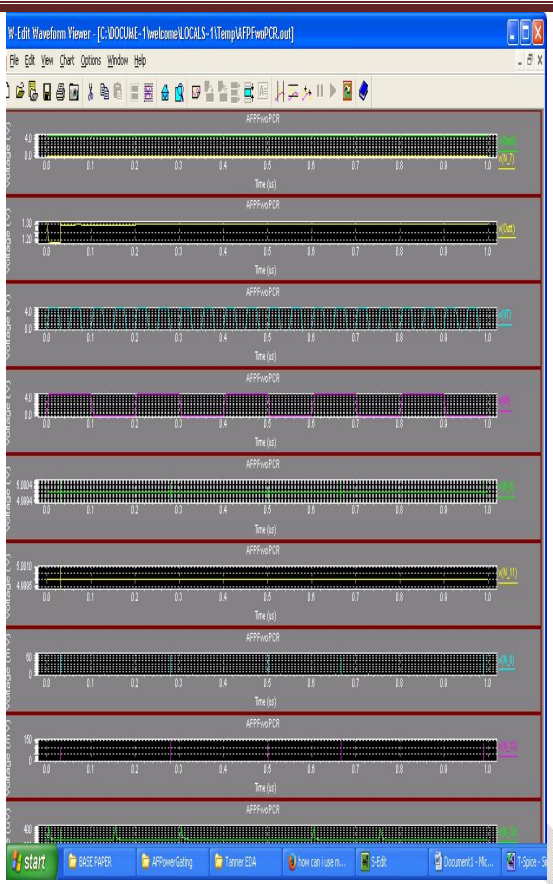

Fig 8 : Output waveform
Input and output voltage in volts with respect to time in microseconds .of Asynchronous Fine Grain Power Gated Logic(AFPL) with PCR.

TABLE.1 POWER ESTIMATION

AVERAGE POWER	
AFPL without PCR	8.860936e-002 watts
AFPL with PCR	5.066655e-002 watts

VII. CONCLUSION

Most digital devices today use synchronous circuits. However asynchronous circuits have the potential to be faster, and may also have advantages in lower power consumption, lower electromagnetic interference, and better modularity in large systems. Asynchronous circuits have an active area of research in digital logic design. Asynchronous circuits designs are much complex. Asynchronous circuits won't switch in inactive mode. Asynchronous circuits in inactive mode have no dynamic dissipation, they still suffer leakage dissipation. In order to reduce the leakage power reduction here implemented the fine grained power reduction technique using the adiabatic logic called Positive Feedback adiabatic Logic (PFAL). Partial Charge Recovery (PCR) mechanism helps to minimize the leakage power dissipation. The design of AFPL with and without PCR was simulated and the power consumption of both circuits was measured using standard T-Spice tool. Result shows the AFPL with PCR mechanism has much reduced power consumption Previously Efficent Charge Recovery Logic(ECRL) is used as basic building unit instead of Positive Feedback Adaibatic Logic(PFAL).

References

[1] Meng-Chou Chang, Member, IEEE, and Wei-Hsiang Chang systems, (june 2013)" asynchronous fine-grain power-gated logic" VOL. 21, IEEE transactions on very large scale integration (vlsi)

[2] C. Ortega, J. Tse, and R. Manohar, .(May 2010,).“Static Proc. IEEE Symp. Asynchronous Circuits Syst.

[3] H. Kawaguchi, K. Nose, and T. Sakurai,(Oct. 2000). “A super cut-off CMOS (SCCMOS) scheme for 0.5 V supply voltage with picoampere stand-by current,” IEEE J. Solid-State Circuits, vol. 35, no. 10, pp. 1498–1501,

[4] J. Tschanz, J. Kao, S. Narendra, R. Nair, D. Antoniadis, A. Chandrakasan, and V. De,(Nov. 2002) “Adaptive body bias for reducing impacts of dieto- die and within-die parameter variations on microprocessor frequency and leakage,” IEEE J. Solid-State Circuits, vol. 37, no. 11, pp. 1396–1402.

[5] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, (Feb. 2003) “Leakage current mechanisms and leakage reduction techniques in deepsubmicrometer CMOS circuits,” Proc. IEEE, vol. 91, no. 2, pp. 305–327,

[6] M. Nomura, Y. Ikenaga, K. Takeda, Y. Nakazawa, Y. Aimoto, and Y. Hagihara, (Apr. 2006)“Delay and power monitoring schemes for minimizing power consumption by means of supply and threshold voltage control in active and standby modes,” IEEE J. Solid-State Circuits, vol. 41, no. 4, pp 805–814,.

[7] S. Mutob, T. Douseki, Y. Matsuya, T. Aoki, S. Shigematsu, and J.Yamada,(Aug.1995) “1 V power supply high-speed digital circuit technology with multithreshold- voltage CMOS,” IEEE J. Solid-State Circuits, vol. 30, no. 8, pp. 847–854.

[8] T. Lin, K.-S. Chong, B.-H. Gwee, and J. S. Chang, (May 2009) “Fine-grained power gating for leakage and short-circuit power reduction by using asynchronous-logic,” in Proc. IEEE Int. Symp. Circuits Syst.

[9] T. Sakurai, (2000) “Boosted gate MOS (BGMOS): Device/circuit cooperation scheme to achieve leakage-free giga-scale integration,” in Proc. IEEE Custom Integr. Circuits Conf. pp. 409–412.

[10] Z. Chen, M. Johnson, L. Wei, and K. Roy, (1998) “Estimation of standby leakage power in CMOS circuits considering accurate modeling of transistor stacks,” in Proc. Int. Symp. Low Power Electron. Design, pp. 239–244.

[11] S. Mutob, T. Douseki, Y. Matsuya, T. Aoki, S. Shigematsu, and J. Yamada, “1 V power supply high-speed digital circuit technology with multithreshold-voltage CMOS,” IEEE J. Solid-State Circuits, vol. 30, no. 8, pp. 847–854, Aug. 1995.